IN THE CLAIMS:

1. (Currently amended) A semiconductor device comprising:

a first interlayer insulating layer;

a plurality of wiring lines which are formed of Cu, said plurality of wiring lines formed on said first interlayer insulating layer;

an insulating layer which has a property that Cu is unlikely to enter said insulating layer and which insulates between said plurality of wiring lines;

a second interlayer insulating layer formed on said insulating layer having a property that Cu is unlikely to enter therein; and

at least one adhesion layer, formed in an interface between said plurality of wiring lines and said insulating layer, for adhering said plurality of wiring lines to said insulating layer,

wherein each said at least one adhesion layer has a polishing rate which is ~~essentially~~ subsequently equivalent to a polishing rate of said plurality of wiring lines.

2. (Previously presented) The semiconductor device according to claim 1, wherein said insulating layer comprises HSQ (Hydrogen Silsesquioxane).

3. (Canceled)

4. (Previously presented) A semiconductor device according to claim 1, wherein a concentration of said Cu is equal to or higher than 10^{19} atoms/cm^3.

5. (Previously presented) The semiconductor device according to claim 4, wherein at least one of said at least one adhesion layer comprises tungsten.

6-13. (Canceled)

14. (Previously presented) A semiconductor device comprising:

a multi-layer insulating layer, comprising:

a middle layer comprised of PAE (Poly Arylene Ether);

an upper insulating layer and a lower insulating layer between which said middle layer is sandwiched, said upper and lower layers each comprised of HSQ (Hydrogen Silsesquioxane); and

an opening formed in a predetermined position in said PAE layer and said HSQ layers; and

a wiring line formed within said opening, said wiring line comprised of Cu having a concentration equal or higher than 10^{19} atoms/cm^3, said upper insulating layer and said lower insulating layer thereby forming an insulating layer which has a property that Cu is unlikely to enter said insulating layer.

15. (Previously presented) A semiconductor device comprising:

a first interlayer insulating layer;

a first layer of low permittivity material formed on said first interlayer insulating layer, said low permittivity material having a property that a migration of copper is limited in said material;

a first plurality of sections of copper being embedded in said first layer of low permittivity material;

a second interlayer insulating layer formed on said layer of low permittivity material,

wherein said first interlayer insulating layer and said second interlayer insulating layer have a property in strength that offsets a property in strength of said first layer of low permittivity material.

16. (Previously presented) The semiconductor device of claim 15, wherein said first interlayer insulating layer and said second interlayer insulating layer each comprise SiN, and

said first layer of low permittivity material comprises hydrogen silsesquioxane (HSQ).

17. (Previously presented) The semiconductor device of claim 16, further comprising:

a bottom layer formed below said first interlayer insulating layer, said bottom layer having at least one copper conductor line,

wherein said first interlayer insulating layer has a hole formed therein, said hole allowing at least one copper conductor line in said bottom layer to connect with one of said first plurality of sections of copper embedded in said first layer of low permittivity material.

18. (Previously presented) The semiconductor device of claim 17, further comprising:

a layer of adhesive material being formed at an interface between said first layer of low permittivity material and each of said first plurality of sections of copper being embedded therein.

19. (Previously presented) The semiconductor device of claim 18, wherein said adhesive material comprises tungsten (W).

20. (Previously presented) The semiconductor device of claim 15, further comprising:

a third interlayer insulating layer formed on said second interlayer insulating layer;

a second layer of low permittivity material formed on said third interlayer insulating layer, said low permittivity material having a property that a migration of copper is limited in said low permittivity material;

a second plurality of sections of copper being embedded in said second layer of low permittivity material; and

a fourth interlayer insulating layer formed on said second layer of low permittivity material.

21. (Previously presented) The semiconductor device of claim 20, wherein said first interlayer insulating layer, said second interlayer insulating layer, said third interlayer insulating layer, and said fourth interlayer insulating layer each comprising SiN, and

wherein said first layer of low permittivity material and said second layer of low permittivity material each comprises hydrogen silsesquioxane (HSQ).

22. (Previously presented) The semiconductor device of claim 20, further comprising:

a layer of adhesive material formed at an interface between said second layer of low permittivity material and each of said second plurality of sections of copper being embedded therein.

23. (Previously presented) The semiconductor device of claim 22, wherein said adhesive material comprises tungsten (W).

24. (Previously presented) The semiconductive device of claim 20, said third interlayer insulating layer has a hole formed therein, said hole allowing a one of said first plurality of sections of copper to connect with one of said second plurality of sections of copper.

25. (Previously presented) A semiconductor device comprising:

a first interlayer insulating layer comprised of a first material;

a middle insulating layer on said first interlayer insulating layer, said middle insulating layer comprising an organic polymer;

at least one copper wiring section embedded in said middle insulating layer; and

a second interlayer insulating layer formed on said middle insulating layer, said second interlayer insulating layer comprised of said first material,

wherein said first interlayer insulating layer, said middle insulating layer, and said second interlayer insulating layer form a system that serves to confine a migration of copper ions from said at least one copper wiring section to be within said middle insulating layer.

26. (Previously presented) The device of claim 25, wherein said first material comprises SiN, and said middle insulating layer comprises hydrogen silsesquioxane (HSQ), said HSQ having a property that a migration of copper ions is limited therein.

27. (Previously presented) The device of claim 25, wherein said first material comprises hydrogen silsesquioxane (HSQ), and said middle insulating layer comprises Poly Arylene Ether (PAE), said HSQ having a property that a migration of copper ions is limited therein so that said first interlayer insulating layer thereby provides a lower layer to confine said migration of copper ions and said second interlayer insulating layer thereby provides an upper layer to confine said migration of copper ions.

28. (Previously presented) A semiconductor device, comprising:

a first interlayer insulating layer;

a plurality of wiring lines which are formed of copper (Cu), said plurality of wiring lines formed on said first interlayer insulating layer;

an insulating layer which has a property that Cu is unlikely to enter said insulating layer and which insulates between said plurality of wiring lines; and

a second interlayer insulating layer formed on said insulating layer having the property that the Cu is unlikely to enter therein,

wherein said insulating layer has a surface region whose Cu concentration is equal to or higher than 10^{19} atoms/cm^3.

29. (Previously presented) The semiconductor device according to claim 28, wherein said insulating layer has an inner region whose Cu concentration is lower than 10^{19} atoms/cm^3.

30. (Previously presented) The semiconductor device according to claim 29, wherein said insulating layer comprises Hydrogen Silsesquioxane (HSQ).

31. (Previously presented) The semiconductor device according to claim 30, wherein a thickness of said insulating layer comprising HSQ is equal to or more than 50 nm.

32. (Previously presented) A semiconductor device, comprising:

a plurality of copper (Cu) wiring lines; and

an insulating layer which insulates between said plurality of Cu wiring lines,

wherein said insulating layer has a surface region whose Cu concentration is equal to or higher than 10^{19} atoms/cm^3.

33. (Previously presented) The semiconductor device according to claim 32, wherein said insulating layer has an inner region whose Cu concentration is lower than 10^{19} atoms/cm^3.

34. (Previously presented) The semiconductor device according to claim 33, wherein said insulating layer comprises Hydrogen Silsesquioxane (HSQ).

35. (Previously presented) The semiconductor device according to claim 34, wherein a thickness of said insulating layer comprising HSQ is equal to or more than 50 nm.

36. (Previously presented) The semiconductor device according to claim 35, wherein said inner region of said insulating layer is an inner region of a position which is 50 nm or more from a surface of said insulating layer.

37. (Previously presented) The semiconductor device according to claim 36, wherein said insulating layer directly contacts Cu.

38. (New) The semiconductor device according to claim 32, wherein:

said insulating layer comprises a multi-layer insulating layer which comprises a middle layer comprised of PAE (Poly Arylene Ether) and an upper insulating layer and a lower insulating layer between which said middle layer is sandwiched, said upper and lower insulating layers each being comprised of HSQ (Hydrogen Silsesquioxane),

openings are formed in predetermined positions in said PAE layer and said HSQ layers, and one of said plurality of said Cu wiring lines is respectively formed in one of said openings, and

said Cu wiring lines comprise Cu having a concentration equal to or higher than 10^{19} atoms/cm^3, said upper insulating layer and said lower insulating layer thereby forming an insulating layer which has a property that Cu is unlikely to enter said upper and lower insulating layers.

39. (New) The semiconductor device according to claim 32, further comprising:

a first interlayer insulating layer formed below said insulating layer; and

a second. interlayer insulating layer formed on said insulating layer,

wherein said first and second interlayer insulating layers have a property in strength that offsets a property in strength of said insulating layer.

40. (New) The semiconductor device according to claim 39, wherein said first and second interlayer insulating layers each comprise SiN, and said insulating layer comprises HSQ (Hydrogen Silsesquioxane).

41. (New) The semiconductor device according to claim 40, further comprising:

a bottom layer formed below said first interlayer insulating layer, said bottom layer having at least one copper conductor line, wherein said first interlayer insulating layer has a hole formed therein, said hole allowing at least one copper conductor line in said bottom layer to connect with one of said plurality of said copper wiring lines.

42. (New) The semiconductor device according to claim 41, further comprising:

a layer of adhesive material formed at an interface between said insulating layer and each of said plurality of copper wiring lines.

43. (New) The semiconductor device according to claim 42, wherein said adhesive material comprises tungsten (W).

44. (New) The semiconductor device of claim 39, further comprising:

a third interlayer insulating layer formed on said insulating layer;

another insulating layer formed on said third interlayer insulating layer, said another insulating layer having a property that Cu is unlikely to enter said another insulting layer;

a second plurality of copper wiring lines formed in said another insulating layer; and

a fourth interlayer insulating layer formed on said another insulating layer.

45. (New) The semiconductor device according to claim 40, wherein said third and fourth interlayer insulating layers each comprise SiN, and said another insulating layer comprises HSQ (Hydrogen Silsesquioxane).

46. (New) The semiconductor device according to claim 44, further comprising:

a layer of adhesive material formed at an interface between said another insulating layer and each of said second plurality of copper wiring lines.

47. (New) The semiconductor device according to claim 46, wherein said adhesive material comprises tungsten (W).

48. (New) The semiconductor device according to claim 44, wherein said third interlayer insulating layer has a hole formed therein, said hole allowing at least one of said copper wiring lines in said insulating layer to connect with one of said second plurality of said copper wiring lines.

49. (New) The semiconductor device according to clam 32, wherein:

said insulating layer comprises a first interlayer insulating layer, a middle insulating layer, and a second insulating layer,

said first interlayer insulating layer comprises a first material,

said middle insulating layer is formed on said first interlayer insulating layer and comprises an organic polymer,

said second insulating layer is formed on said middle insulating layer and comprises a first material,

said first interlayer insulating layer, said middle insulating layer, and said second insulating layer form a system that serves to confine a migration of copper ions from said copper wiring lines to be within said middle insulating layer.

50. (New) The semiconductor device of claim 49, wherein said first material comprises SiN, and said middle insulating layer comprises hydrogen silsesquioxane (HSQ), said HSQ having a property that a migration of copper ions is limited therein.

51. (New) The semiconductor device of claim 50, wherein said first material comprises hydrogen silsesquioxane (HSQ) and said middle insulating layer comprises Poly Arylene Ether (PAE), said HSQ having a property that a migration of copper ions is limited therein, so that said first interlayer insulating layer thereby provides a lower layer to confine said migration of copper ions and said second interlayer insulating layer thereby provides an upper layer to confine said migration of copper ions.